In The Claims:

Please amend the claims as follows:

1. (Previously Presented) A device for fault testing in a microprocessor chip comprising:

a test unit for receiving a first reference signature indicative of faults at a first frequency;

a loading unit responsive to the test unit for receiving and outputting masking data; and

a masking unit coupled to the loading unit, the masking unit generating a second reference signature responsive to the masking data and scanning data from a scan string in the chip, wherein the second reference signature replaces the first reference signature such that the test unit is responsive to faults at a second frequency.

2. (Previously Presented) The device for fault testing of claim 1 further comprising a masking register file connected between an output of the loading unit and an input of the masking unit, wherein the masking register file feeds back the masking data to the loading unit for saving a reloading time after the testing.

3. (Previously Presented) The device for fault testing of claim 2, wherein the masking register file further comprises multiple latches, wherein the number of latches of the masking register file is equal to or greater than the number of latches in the scan string on the chip.

4. (Previously Presented) The device for fault testing of claim 2, wherein the masking register file includes a scan-only register.

5. (Previously Presented) The device for fault testing of claim 2, wherein the masking register file performs an exclusive testing to a predetermined latch.

6. (Currently Amended) The device for fault testing of claim 5, wherein the latches of the masking register file shift bit-by-bit in ~~sychronization~~synchronization with latches in the scan string, respectively, in response to a clock.

7. (Previously Presented) The device for fault testing of claim 2 further comprising a control unit connected between an output of the masking register file and the input of the masking unit, wherein the control unit controls the masking register file to withhold the masking data for saving a loading time during the testing.

8. (Currently Amended) The device for fault testing of claim 7, wherein the control unit ~~includes~~ is an OR gate.

9. (Original) The device for fault testing of claim 1, wherein the masking unit assigns a predetermined value to a failing latch in the scan string for identifying a location and a test frequency of the failing latch.

10. (Currently Amended) The device for fault testing of claim 1, wherein the masking unit ~~includes~~ is an AND gate.

11. (Original) The device for fault testing of claim 1, wherein the loading unit is a multiplexor.

12. (Previously Presented) A method for fault testing in a microprocessor chip comprising the steps of:

generating a first reference signature indicative of faults at a first test frequency;

testing the first reference signature with a target signature;

identifying a failing pattern if the first reference signature is not equal to the target signature;

masking the failing pattern based on masking data and scanning data from a scan string in the chip; and

replacing the first reference signature by a second reference signature responsive to a fault at a second test frequency.

13. (Original) The method for fault testing in a microprocessor chip of claim 12, wherein the step of masking the failing pattern further comprises the step of withholding the masking data for saving a loading time during the testing.

14. (Previously Presented) The method for fault testing in a microprocessor chip of claim 13, wherein the step of masking the failing pattern further comprises the step of

shifting the masking data in synchronization with the scanning data bit-by-bit for matching the reference signature with the target signature.

15. (Original) The method for fault testing in a microprocessor chip of claim 13, wherein the step of masking the failing pattern further comprises the step of assigning a given value for a failing pattern for identifying a location and a test frequency of the failing pattern.

16. (Previously Presented) The method for fault testing in a microprocessor chip of claim 12, wherein the step of masking the failing pattern further comprises the step of feeding back the masking data to a loading unit for saving a reloading time after the testing.

17. (Currently Amended) The method for fault testing in a microprocessor chip of claim 12, wherein the step of masking the failing pattern comprises masking a ~~predetermeined~~predetermined latch for exclusively performing testing of scan data corresponding to said latch.

18. (Currently Amended) A method of determining a worst failing frequency for a first portion of a chip with a known latch failure pattern at a reduced failing frequency for a second portion of the chip, comprising the steps of:

loading a masking data set indicative of the known latch failure pattern;

~~over riding~~overriding use of said masking data set for determining the reduced

failing frequency of the second portion;

generating a first reference signature indicative of the second portion faults at the reduced failing frequency;

testing said first reference signature with a target signature;

identifying a failing pattern if the first reference signature is not equal to the target signature;

removing the ~~over ride~~override to allow use of said masking data set;

masking the failing pattern of the second portion based on said masking data set;

scanning data from a scan string in said chip indicative of a failure pattern in the first portion; and

replacing said first reference signature by a second reference signature responsive to a fault at the worst failing frequency.